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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,974	07/07/2003	Chandra Mouli	M4065.0941/P941	4728

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EXAMINER
ABRAHAM, FETSUM

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	10/612,974	MOULI, CHANDRA	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,39 and 42-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *all* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The election made on 11/9/05 has been acknowledged and considered. The arguments traversing the restriction requirement have also been considered but fond moot to change the situation. The decision to declare extend of burden on examination imposed by claims of different scope is mainly that of the examiner's, and in this particular case, a photosensor as an element does not need the other elements (reset transistor, source follower transistor, row select transistor and transfer transistor). A photo sensor can be any element that senses light and such element can be a diode, any photoelectric transducer such as photransistor individually. Clearly, the concept of invention changes when the claimed other elements are included, because now there is an array of structures or matrix of elements in display device. The individual elements are classified differently (257//79,82) from that of the matrix structure classified in 9257//59,72). This is only an example of classification difference within a class but the classification can change dramatically when other optical classes in the PTO system are involved.

In view of the fact that examination burden is imposed if all claims are examined the examiner believes that adequate reasoning is provided to sustain the restriction requirement. Therefore, the non-elected claims have been withdrawn from consideration.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,7,39,42,43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freedman et al (Integrated SiGe and Si device capabilities and trends for multi-gigahertz applications).

As for claims 1,3,39,43 the applicant submitted document discloses a structure in figure 13 comprising a strained silicon layer on SiGe base material for FET construction on the upper surface of the structure but omits to discus she TFT as being a phgotosensor device. However, TFTs indeed are pohotosensors for the following realistic capacities:

a) TFTs in optical applications are usually protected from radiation-induced damages by shielding layers over their active regions.

b) TFTs are photosensitive structures in view of the reason in (1).

c) The capacity of the active layers of MOSFETs characterized by bipolar structures (source/channel/drain) that are either PNP or NPN devices) functioning as phototransistors renders photo-detection an integral character of MOSFETs. To explain the concept a little deeper, light is directed to the base (channel) layers of a

phototransistor to generate base current that is readable at the collector (drain) level of such structures. In such applications, light is detected at the channel and transduced into electrical signal to be collected at the drain of any known semiconductor MOSFET structures.

Therefore, although the light detection nature of the TFT in the prior art is not as such taught because of the dominant subject matter of the project (high frequency devices), the claimed photo detection is covered by the TFT on the silicon layer for one skilled in the art to safely relate the prior art with the claimed invention.

As for claims 2,42, the specification discusses the claimed thickness as the following:

Detail Description Paragraph:

[0031] The strained silicon layer 170 has, for example, a thickness of about 500 .ANG. to about 1000 .ANG.. It should be noted, however, that the thickness could vary by forming a relaxed SiGe top layer over a graded bottom SiGe layer as a composite stack.

Clearly, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, the claimed thickness is arbitrary and cannot be considered as patentable without criticality.

As for claims 4,7,44,48 material composition of a compound is a function of material effect dominance. Such composition percentages are notoriously known variables in the art. In this case, it would have been obvious to one skilled in the art to have the silicon concentration in the SiGe compound more than that of the Germanium to minimize lattes mismatch induced problems with the silicon layer on the SiGe base layer.

In general, material composition in a given compound is variable and "material effect" dependent that has no patentable weight.

As for claim 39, the prior art structure is formed by the claimed method.

Claims 5,45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freedman et al (Integrated SiGe and Si device capabilities and trends for multi-gigahertz applications) in view of Noguchi et al (6,819,592).

The primary reference discloses all subject matter claimed but a SiGeC substrate as alternative to the SiGe substrate. However, the secondary reference fills the gap in view of the following teaching:

Detailed Description Text (265):

While the p type S1 substrate is used as the semiconductor substrate in the embodiments, an n type S1 substrate or an SOI substrate may be used. Further, the other silicon-containing monocrystalline semiconductor substrate such as an SiGe mixed crystal substrate or an SiGeC mixed crystal substrate may be used. Further, the gate electrode can be formed out of silicide or polycide such as SiGe mixed crystal, SiGeC mixed crystal, TiSi, NiSi, CoSi, TaSi, WSi or MoSi, metal such as Ti, Al, Cu, TiN

or W, polycrystalline material, or the layered structure thereof. The charge accumulation layer may be formed in the form of dots.

Note that the substrate is layer (21) in the front-page figure. Therefore, it would have been obvious to one skilled in the art to replace the SiGe substrate in the primary reference with the SiGeC substrate of the secondary reference in order to provide the primary structure with the benefits of carbon material properties.

Ad for the X+Y+Z = 1 in the claim language, the chemical total atomic concentration of any compound converges to 100% or 1.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freedman et al (Integrated SiGe and Si device capabilities and trends for multi-gigahertz applications) in view of Buchanan et al (6,984,591).

The primary reference discloses all subject matter claimed but a multilayered substrate. The secondary reference, however, fills the gap by stating the following:

27. The method of claim 12 wherein the substrate is selected from the group consisting of semiconductor substrates, dielectrics, metals, organic substrates, glasses, metal oxides, and plastic polymeric substrates, Si-containing semiconductor substrates, ceramics, silicon-on-insulator substrates, Ge substrates, SiGe substrates, GaAs substrates, and mixtures or multilayers thereof.

As for the variable Ge concentration in the claim, the concept of atomic concentration in given compound has already been discussed above.

Therefore, it would have been obvious to one skilled in the art to use a multilayer

substrate in the primary reference product since such structures are more reliable and stronger than those formed on single layered substrates.

Claims 46,47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freedman et al (Integrated SiGe and Si device capabilities and trends for multi-gigahertz applications) in view of Pomarade et al (6,613,695).

The primary reference discloses all subject matter claimed but the method of forming the silicon layer on the SiGe base material. However, the secondary reference teaches the following:

Detailed Description Text (4):

As noted in the Background section above, many deposition processes are sensitive to the surface over which deposition is required. Doped polysilicon and polycrystalline silicon-germanium alloy (poly-SiGe) tend to nucleate poorly over silicon oxide, as is well known in the art, and also over newer high-k materials now being investigated. The present invention provides a method for preparing the dielectric surface for electrode deposition thereover, advantageously without significant deposition and preferably without significant modification of bulk properties of the dielectric.

Detailed Description Text (6):

Unfortunately, depending upon the chemistries employed, ALD does not deposit equally well on different starting substrates. Some ALD process recipes, for example, have been found slow or even non-operative in depositing over silicon, and particularly etched or cleaned silicon surfaces (typically hydrogen-terminated). For example, it is

unlikely that aluminum alkyls, such as (CH.sub.3).sub.3 Al, can attach on a hydrogen-terminated silicon surface in ALD processes for depositing Al.sub.2 O.sub.3.

Detailed Description Text (32):

Additional source gases include an ammonia (NH.sub.3) source (not shown), which serves as a volatile nitrogen source, useful in CVD and nitridation anneal steps. A silicon source 86 is also provided, illustrated as monosilane (SiH.sub.4). As is known in the art, silanes, including monosilane (SiH.sub.4), disilane (Si.sub.2 H.sub.6), trisilane (Si.sub.3 H.sub.8), DCS and TCS, are volatile silicon sources for CVD applications, such as the deposition of poly-SiGe, silicon nitride, metal silicides, and extrinsic or intrinsic silicon (polycrystalline, amorphous or epitaxial, depending upon deposition parameters). Monosilane (SiH.sub.4), as illustrated, is particularly preferred to avoid chlorine incorporation into sensitive gate dielectric structures.

Detailed Description Text (56):

Like the excited species treatment 110 preceding ALD, the treatment 125 preceding silicon or poly-SiGe deposition modifies the surface termination of the substrate to promote subsequent deposition. Advantageously, the treatment 125 is tuned such that the excited species impart sufficient activation energy to break the surface bonds and form new ones, while process parameters are tuned to maintain energy levels low enough to prevent etching of the substrate or significant diffusion of active species into the bulk material of the gate dielectric. Additionally, no appreciable deposition takes

place. At the most, a monolayer of terminating tails is left by the excited species treatment 125. However, the process can be tuned to convert the topmost few monolayers of high k oxide to nitride by breaking metal-oxygen bonds and replacing them with metal-nitrogen bonds. Preferably, temperatures are kept between about room temperature and 800.degree. C.

Therefore, it would have been obvious to one skilled in the art to deposit the silicon layer of the prior art by CVD method since the method produces dependable and layer at relatively faster rate and since the method produces chlorine free gate structures in MOSFET production.

Furthermore, it would have been obvious to one skilled in the art to deposit the silicon layer of the prior art by ALD means since the method provides ultra thon layers suitable for thin film products.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Refer to PN: 6,583,015.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
2/10/06